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Direct communication between magnetic tunnel junctions for nonvolatile logic fan-out architecture

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We experimentally demonstrated a magnetic tunnel junction (MTJ) based circuit that allows direct communication between elements without intermediate sensing amplifiers. The input of the circuit consists of three MTJs connected in parallel. The direct communication is realized by connecting the output in series with the input and applying voltage across the series connections. Combining the circuit with complementary metal oxide semiconductor current mirrors allows for fan-out to multiple outputs. The change in resistance at the input resulted in a voltage swing across the output of 150–200 mV for the closest input states which is sufficient to realize all of the Boolean primitives. © *2010 American Institute of Physics*. [doi:10.1063/1.3499427]

State-of-the-art complementary metal oxide semiconductor (CMOS) logic devices are facing challenges such as increased power dissipation and device variability, which has created a strong demand for alternative or hybrid technologies. Magnetic tunnel junction (MTJ) and giant magnetoresistance are magnetoresistive (MR) devices, which store and process information based on the relative orientation of two thin magnetic layers separated by a nonmagnetic layer.[1] These MR devices are an attractive technology since they are nonvolatile, low power, high speed, high density, and reprogrammable.[1–3] MTJs have also been integrated with CMOS in commercially available magnetic random access memory.[4]

A significant amount of reprogrammable logic circuits based on MR devices[5–21] have been proposed and demonstrated which realized the primitive Boolean logic operations[5] and more advanced components such as hybrid flip-flops,[18,19] static random access memory,[20] and full adders.[12,21] However, these previous circuits required every MR element to be read using a sense amplifier. Then the information is passed on to the next stage of circuitry. The need for this intermediate circuitry hinders fan-out function, adds integration complexity, power consumption, area, and delay overhead to logic modules, and hence their need must be minimized to gain a full advantage of the spintronic technology.

To address these drawbacks, designs have been proposed which connect MR devices together using magnetic layers.[22–24] While similar structures have been fabricated,[25] a logic circuit and communication between multiple MR devices is yet to be realized. In this study, we have designed and fabricated an MTJ based logic circuit which connects multiple MTJs to realize direct communication. The circuit simultaneously performs a logic computation while transferring the data to the next logic gate without an intermediate sense amplifier. This MTJ logic circuit can perform majority, AND, OR, NAND, and NOR operations. The design utilizes current to switch the output MTJ using spin torque transfer (STT) switching.[26,27] We supplemented the experimental demonstration with a SPICE simulation of the MTJ circuit combined with CMOS. The simulations verified that fan-out to multiple outputs can be realized using CMOS current mirrors. The combination of simultaneous computation and communication without the need for intermediate sensing amplifiers allows complex and multistage logic to be realized.

The MTJ devices have a multilayered structure as follows: Si substrate/SiO_2(100 nm)/bottom lead/PtMn (20 nm)/$Co_{70}Fe_{30}$(2.4 nm)/Ru (0.85 nm)/$Co_{60}Fe_{20}B_{20}$ (2.4 nm)/MgO (1.05 nm)/$Co_{60}Fe_{20}B_{20}$(1.6 nm)/top lead. The devices were patterned into an ellipse shape using e-beam lithography followed by an ion milling process. The transport measurements were carried out sourcing current and magnetic fields. For all of the STT switching measurements the dipole field on the free layer was canceled out by applying an external magnetic field. The positive current is defined as the electrons flow from the fixed layer into the free layer. The direction of positive magnetic fields is defined as the direction opposite to the magnetization in the fixed layer. The tunneling magnetoresistance ratio (TMR) is about 50%. The product of the resistance and area (RA) values for a parallel state is approximately 10–12 $\Omega\ \mu m^2$.

Figures 1(a) and 1(b) show a schematic of the basic logic device and an optical image of the fabricated device, respectively. Three MTJs are connected in parallel at the input with a single MTJ connected at the output. The input and output are connected in series to form a voltage divider which allows the information from the input to be passed to the output MTJ. All of the MTJs were designed to have the same resistance. The resistance states at the input for one MTJ AP, two AP, and three AP are defined as 001, 011, and 111, respectively [Fig. 1(a) shows the 111 state and the 100 state]. However, the aspect ratio of MTJs was varied in order to change the coercivity so different resistance states could be set with an external magnetic field as shown in Fig. 2(a). The aspect ratios of the input MTJs were 2.0, 2.5, and 3 which corresponds to a coercivity of the CoFeB free layer of approximately 22 Oe, 50 Oe, and 70 Oe, respectively. The inset in Fig. 2(a) shows the MR field switching measurements for the output MTJ. The aspect ratio of the output was set to

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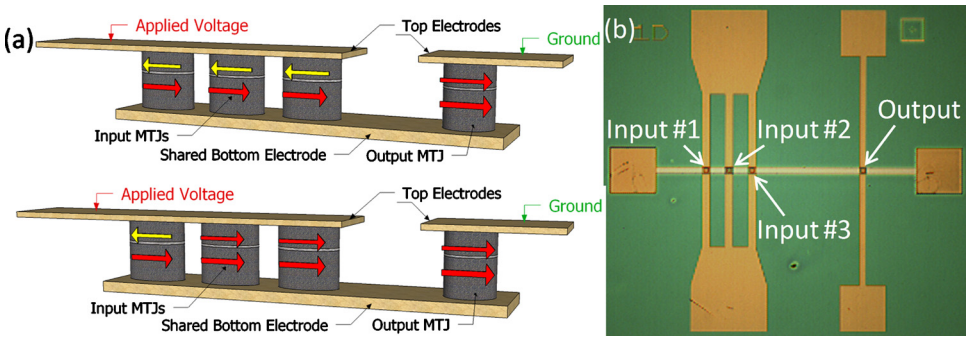

FIG. 1. (Color online) (a) Working principle of the circuit with three MTJs connected in parallel to form the input and connected in series with the output to form the voltage divider circuit, (b) optical image of the top view of the fabricated device.

1.4 which allows the MTJ to be easier to switch while maintaining thermal stability. The dimensions of the output was 238 nm × 357 nm; the input MTJs were 190 nm × 380 nm, 162 nm × 405 nm, and 142 nm × 426 nm, respectively.

With the voltage applied across the output only, a clear antiparallel (AP) to parallel (P) switch is observed at a voltage of 0.98 V, which corresponds to a current density of 7.5×10^6 A/cm^2. During the logic measurement, the voltage is applied across the series connection of the input and output. Figure 2(b) shows the AP to P STT switching of the output for three different input states. Changing the input state causes a shift in the voltage required to switch the output. A 150–200 mV separation in switching voltages occurs for progressive input states, which provides a sufficient range for application purposes. Similar results are observed for P to AP switching.

During initial characterization, the applied voltage was swept to determine the switching voltage for various inputs. However, for logic application, the voltage is held constant. For example, the majority function can be realized by presetting the output to 1. Then, a voltage is selected so that when the majority of the inputs are 1, there is insufficient current to switch the output to 0. When the majority of the inputs are 0 (low resistance) sufficient current is supplied to switch the output to 0. The operating voltage is determined by examining the location of the knees in Fig. 2(b). For the majority functions, the operating voltage should be set between the knees of the 001 and 011 inputs. When similar reasoning is applied, the AND, OR, NAND, and NOR logic functions can be realized. Table I shows a truth table for the logic operations the MTJ circuit was able to perform, the required initial sate of the output, and operating voltages.

For this experimental demonstration, field switching was used to set the input resistance states. However, when this design is combined with CMOS, the three inputs can be set individually using STT switching. This would allow all of the input states to be set (e.g., 101, 010, 110, and so on). CMOS also provide the possibility of fan-out to multiple outputs using current mirrors.[28] The implementation of fan-out in MTJ based logic is well known as a long-standing and difficult challenge.

Figure 3(a) shows a schematic of the MTJ logic circuit combined with a CMOS current mirror used for the fan-out simulations. The hybrid MTJ/CMOS circuit was simulated in HSPICE using our previously developed model.[29] The voltage and MTJ sizes were scaled to match the output impedance of the 45 nm CMOS[30] and the TMR was increased to 200%.[31] For the simulations, CMOS current mirrors are used to fan-out to three outputs; however it could be expanded to many more. A 0.8 V pulse was applied to the circuit for 50 ns to simulate a majority gate. The voltage pulse is applied at 10 ns which causes a small drop in resistance. Figure 3(b) shows that for the 001 input state, all three outputs switch to 0. However, when the input is 011, all three outputs remain 1 as shown in Fig. 3(c). The variation in switching times for the outputs is due to a 5% random distribution of device sizes. The simulation used 50 ns pulses because it provided good switching margins, however, we were able to operate the device down to a 5 ns pulse but device margins became very small. Future developments in ultrafast switching may improve the margins, allowing for faster operation.

The significance of the three input design is that it realizes the majority function in addition to the basic logic operations. The majority function has been demonstrated to be a universal logic operation,[32] which means that using only the majority functions, all other Boolean primitives can be derived. The majority function has been understudied in CMOS logic due to its inefficient implementation; however, it is very natural to realize using MTJs.

In conclusion, this MTJ design was demonstrated to perform all the primitive logic functions and simultaneously

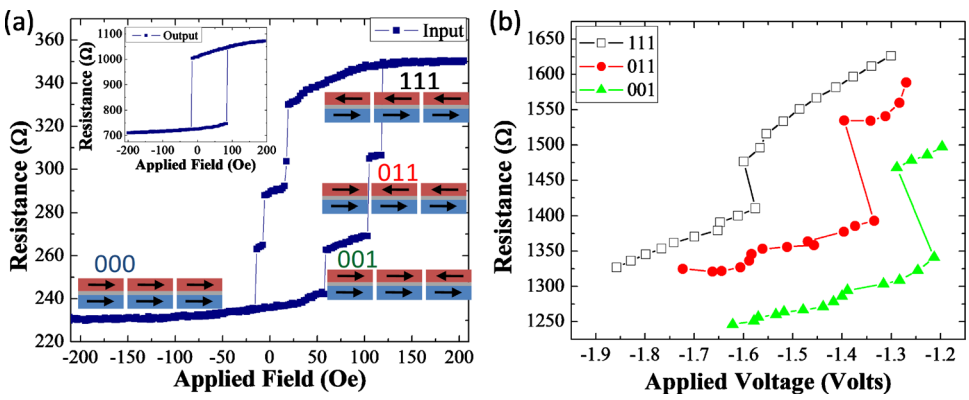

FIG. 2. (Color online) (a) Field switching loop of the input with the different resistance states defined as logic states. (Inset shows output MR loop) and (b) current switching of the output MTJ for three different resistance states of the input.

TABLE I. Truth table for the realized logic functions.

	Function output				
Input state	Majority	AND	OR	NAND	NOR
000	0	0	0	1	1
001	0	0	1	1	0
010	0	0	1	1	0
011	1	0	1	1	0
100	0	0	1	1	0
101	1	0	1	1	0
110	1	0	1	1	0
111	1	1	1	0	0
Initial state	1	1	1	0	0
Set V	−1.3	−1.5	−1.1	1.5	1.1

pass the information to the output without a sensing circuit. Removal of the sense amplifier and implementation of the fan-out function is a breakthrough step in making MTJ based logic the forerunner as a replacement for CMOS logic. As MTJs become a more central part of a processor their advantages can be fully realized.

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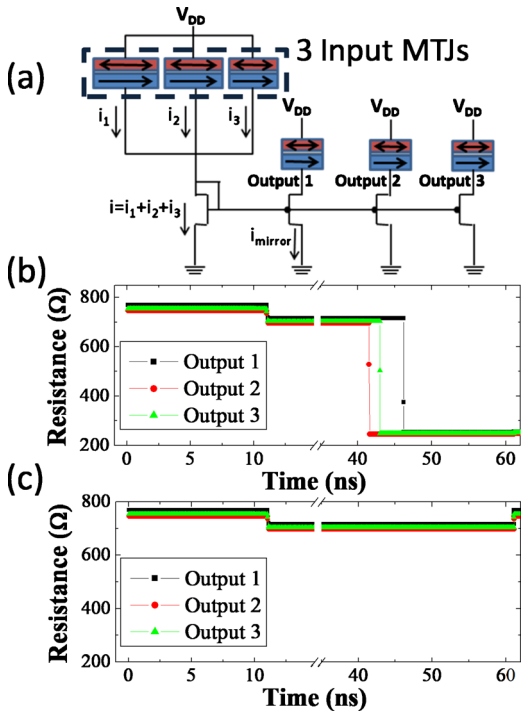

FIG. 3. (Color online) (a) Schematic of the MTJ logic and CMOS current mirror circuit and majority gate simulation results showing fan-out to three different MTJ outputs using CMOS for (b) 100 and (c) 110 input states.

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