A Spintronics Full Adder For Magnetic CPU

Hao Meng, Jianguo Wang, and Jian-Ping Wang

***Abstract*—Spintronics devices are based on the up or down spin of the electrons rather than on electrons or holes as in the traditional semiconductor electronics devices. Magnetic processors using spintronics devices in principle are much faster and with the potential features of nonvolatile, lower power consumption and higher integration density compared with transistor-based microprocessor. Full adder is one of the most important basic units of the arithmetic/logic unit for any processors. The design of the full adder determines the speed and chip-density of a processor. In this paper, a novel spintronics full adder is proposed based on novel programmable spintronics logic devices. Only seven magnetic tunnel junction elements are needed for this full adder design.**

***Index Terms*—Full adder, magnetic CPU, magnetic tunnel junction, magnetoresistance, magnetic random access memory (MRAM), programmable, spintronics logic device.**

I. Introduction

A CENTRAL processing unit (CPU) of a computer is the complete computation engine that is fabricated on a single chip based on the transistor technology [1]. Over the past several decades, the computing power of modern computers has been dramatically increased, by shrinking transistor dimension and chip's circuitry [2]. However, this method is approaching its physical limitations [3]. Researchers never stop looking for new devices or new methods for future computers, such as spintronics computing, single electron transistor (SET), molecular electronic RTD, and nano-CMOS [4]–[13], [32], [33]. Recently, more and more attention has been paid to spintronics computing [14]–[19]. Spintronics devices are based on the up or down spin of the electrons rather than on electrons or holes as in the traditional semiconductor electronics devices. Recently, the concept of a magnetic processor based on a spintronics device has been mentioned [20], [21], which could have the features of faster computing, nonvolatile, superior heat-dissipation, and high-density integration compared with the transistor-based processors. However, there is no implemental concept published on this topic yet. Since full adder is the base of the arithmetic/logic unit for any processors [22], in this paper, a new programmable spintronics full adder has been designed by using only seven magnetic tunnel junctions (MTJs).

II. Device Design

Spintronics devices, such as the spin dependent MTJ [23], [24], are well developed for magnetic sensors, read heads, and magnetic random access memory applications due to its high magnetoresistance ratio, high sensitivity and current-perpendicular-to-the-plane (CPP) configuration [25]–[27]. The resistance of an MTJ element depends on the relative magnetization orientation of free and pinned layers. It is lower for their parallel alignment and higher for their antiparallel alignment. These two resistance states can be identified with logical 1 and 0, respectively. Furthermore, only the free layer's magnetization orientation could be changed by magnetic field generated from the current line(s). In Fig. 1(a), the high (logic 1) and low resistance (logic 0) can be obtained by passing "positive" current (logic 1) and "negative" current (logic 0) through line A, respectively. The resistance (logic state) of logic element shown in Fig. 1(b) depends on three input lines A, B, and C. If more than two input lines are passing "positive" current, the resistance is high. If more than two input lines are passing "negative" current, the resistance is low. The magnetization directions for all layers are remained even without current. The logical information is nonvolatile and can be read out repeatedly by measuring the resistance of the MTJ element without the periodic refreshing. Fig. 1(c) and (d) shows the schematics of a logic element in Fig. 1(a) and (b), which will be used in the following drawings. In this letter, we describe a novel hardware concept for a spintronics full adder just based on seven above MTJ elements.

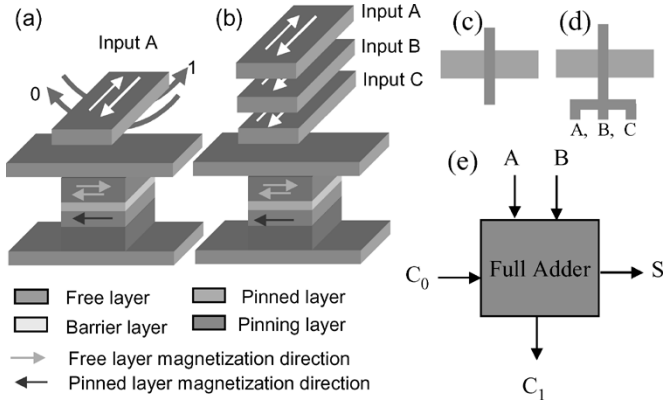

Fig. 1. Schematics of a logic MTJ element. (a) With one input line, (b) with three input lines, (c) simpler schematics of logic MTJ element with one input line, (d) simpler schematics of logic MTJ element with three input lines, and (e) schematics of one bit full adder with three inputs (A, B, C_0) and two outputs (S, C_1).

The schematic of a standard one bit full adder is shown in Fig. 1(e). A and B are the adder inputs, C_0 the carry input, *S* the sum output, and C_1 the carry output, respectively. The Boolean expressions for S and C_1 are given as

$$\mathrm{S}=\mathrm{A}\ \boldsymbol{XOR}\ \mathrm{B}\ \boldsymbol{XOR}\ \mathrm{C}_0 \quad (1)$$

$$\mathrm{C}_1=(\mathrm{A}\ \boldsymbol{AND}\ B)\,OR\,(A\ \boldsymbol{AND}\ \mathrm{C}_0)\,OR\,(\mathrm{B}\ \boldsymbol{AND}\ \mathrm{C}_0). \quad (2)$$

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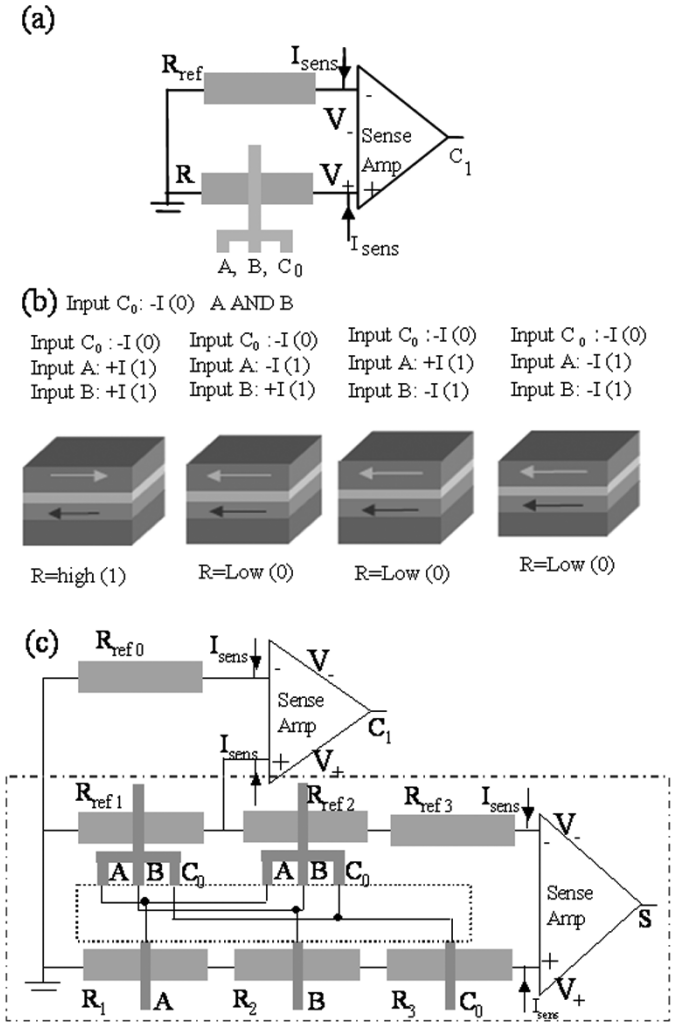

Fig. 2. (a) Circuit design for spintronics full adder carry output C_1 logic function. (b) Principle of AND gate operation between input A and B when carry input C_0 is logic 0. (c) Circuit design for spintronics full adder. Circuit inside the dash line: the sum output (*S*) logic functions.

Equations (1) and (2) can be described in detail as the following:

When the input carry C_0 is 0, S and C_1 can be expressed as

$$\mathrm{S} = \mathrm{A}\ \boldsymbol{XOR}\ \mathrm{B} \tag{3}$$

$$\mathrm{C}_1 = \mathrm{A}\ \boldsymbol{AND}\ \mathrm{B} \tag{4}$$

When the input carry C_0 is 1, S and C_1 can be expressed as

$$\mathrm{S} = \mathrm{A}\ \boldsymbol{XNOR}\ \mathrm{B} \tag{5}$$

$$\mathrm{C}_1 = \mathrm{A}\ \boldsymbol{OR}\ \mathrm{B}. \tag{6}$$

Fig. 2(a) shows the circuit design using the MTJ elements for a carry output. The bottom MTJ element with three separated inputs (A, B, C_0) is operated as a logic-active element, and the top MTJ element is low resistance state as a reference resistor. For a logic output reading, same sensing currents (I_{sense}) pass through the logic-active and reference MTJ elements. The difference of the voltage from the bottom (V_+) and the top (V_-) MTJ elements can be expressed as

$$\mathrm{V}_+ - \mathrm{V}_- = I^*_{\mathrm{sense}} R_- - I^*_{\mathrm{sense}} R_{\mathrm{ref}} = I^*_{\mathrm{sense}}(R_- - R_{\mathrm{ref}}). \tag{7}$$

The logic output depends on the resistance state of the logic-active MTJ element. If the resistance of the logic-active MTJ is high, the logic output of carry C_1 is high (logic 1), otherwise the carry C_1 logic output is low (logic 0). Fig. 2(b) shows the Boolean operation of A AND B logic function for three inputs logic MTJ element. If the carry input C_0 is set to logic 0 (passing "negative current"), only when the inputs A and B are set to logic 1 (passing "positive current"), the resistance of logic MTJ is high, and the carry C_1 output of logic is 1. Otherwise the resistance of logic MTJ is low, and the logic output is 0. When the input C_0 is set as logic 1 (passing "positive current"), only when both inputs A and B are set as logic 0 (passing "negative current") the resistance of the logic MTJ is low, and the output of carry C_1 is 0. Otherwise the logic output is 1. So the logic function is OR between inputs A and B when the carry C_0 is 1. According to (4) and (6), the logic circuit shown in Fig. 2(a) used two MTJ elements can realize logic functions of full adder carry output C_1.

Fig. 2(c) (inside the dash line square) shows the circuit structure for a spintronics full adder sum S output. In this configuration, the bottom bits are the logic-active MTJ elements with one input line for the inputs A, B and the carry input C_0, and the top bits are the reference bits. Two of the reference bits are logic-active MTJ elements with three inputs, whose resistance also depend on the inputs A, B and the carry input C_0. The other reference bit is the same MTJ element with low resistance state as a reference. The voltage difference between V_+ and V_- can be expressed as below

$$\begin{aligned}\mathrm{V}_+ - \mathrm{V}_- &= I^*_{\mathrm{sense}}(R_1 + R_2 + R_3) - I^*_{\mathrm{sense}}(R_{\mathrm{ref1}} + R_{\mathrm{ref2}} + R_{\mathrm{ref3}}) \\ &= I^*_{\mathrm{sense}}\left((R_1 + R_2 + R_3) - (R_{\mathrm{ref1}} + R_{\mathrm{ref2}} + R_{\mathrm{ref3}})\right).\end{aligned} \tag{8}$$

When the carry input C_0 is 0, the logic function between the input A and B is XOR. If both the input A and B are 1 (or 0), R_1, R_2, R_3 and R_{ref1}, R_{ref2}, R_{ref3} are 1, 1, 0 (or 0, 0, 0) the logic output is 0. If only one of input A and B are 1, the reference bits are 0, 0, 0, and the bottom logic bits are 0, 1, 0 or 1, 0, 0, so the logic output is 1. Similarly, the logic function between input A and B is XNOR when the carry input C_0 is 1. According to (3) and (5), the circuit structure as shown in Fig. 2(c) inside the dash square can realize the sum S output logic functions for a full adder. By integrating a carry output circuit as shown in Fig. 2(a) with a sum output circuit, a complete spintronics full adder circuit structure is achieved, as shown in Fig. 2(c). The R_{ref1} is not only the reference MTJ element for sum *S* output logic function but also the logic element for carry C_1 output logic function.

III. Experiment

The basic functions needed in the full adder are XOR, OR, etc, in the above discussion. A prototype was fabricated to demonstrate XOR and OR functions based on a single MTJ element. A Wheatstone bridge composed by four MTJ elements was engineered as shown in Fig. 3(a). Three of the four MTJ elements function as references with low resistance while the fourth is the logic-active device. When the active MTJ element is with low (logic 0) or high (logic 1) resistance, the bridge output is with low or high voltage, respectively. The detailed device design and input line functions, parameters have been reported in our previous work [28], [29]. Fig. 3(b) shows the logic gate of XOR and OR operation. A voltage

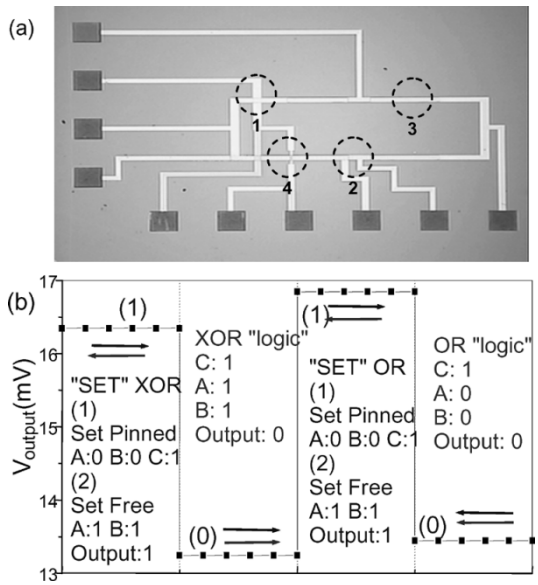

Fig. 3. (a) Image of the prototype diagram of magnetic logic devices. The dash circles show the location of the four MTJs, the fourth one is the logic active MTJ element. (b) Experimental data of logic functions XOR and OR.

with 1 V is applied across the Wheatstone bridge. The first step is XOR gate "SET." By setting input A, B, and C as 0, 0, and 1 and followed by 1, 1,and 0, the magnetization directions of the pinned layer and the free layer are antiparallel. The logic-active MTJ element has high resistance, and bridge has output 16.4 mV (logic 1). The second step is the XOR gate "logic." When input A, B, and C are 1, 1, and 1, the magnetization directions of the free layer and pinned layer become parallel. The logic-active MTJ element has low resistance and the bridge has output 13.2 mV (logic 0). The third step is OR gate "SET." By setting input A, B, C as 0, 0, and 1 and followed by 1, 1, and 0, the magnetization directions of the pinned layer and free layer are antiparallel. The logic-active MTJ element has high resistance and the bridge has output 16.8 mV (logic 1). The fourth step is OR gate "logic." When input A, B, and C are 0, 0, and 1, the magnetization directions of the free layer and pinned layer become parallel. The logic-active MTJ element has low resistance and the bridge has output 13.2 mV (logic 0). The 13.2-mV voltage is the offset of the bridge. About 3-mV output difference is obtained between logic 1 and 0. The output signal could be improved by increasing MR ratio. For example, if use MgO as the barrier layer, the MR ratio could be up to 220% at room temperature [30], [31]. This will greatly increase the logic device output signal. Smaller device and optimized circuits design are ongoing to lower operation power and increase integration density.

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